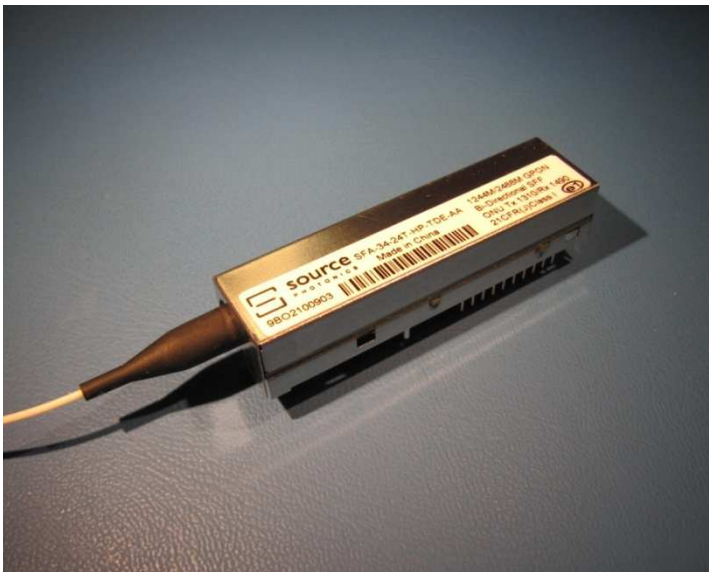
SFX-34-24T-HP-XDH-XX



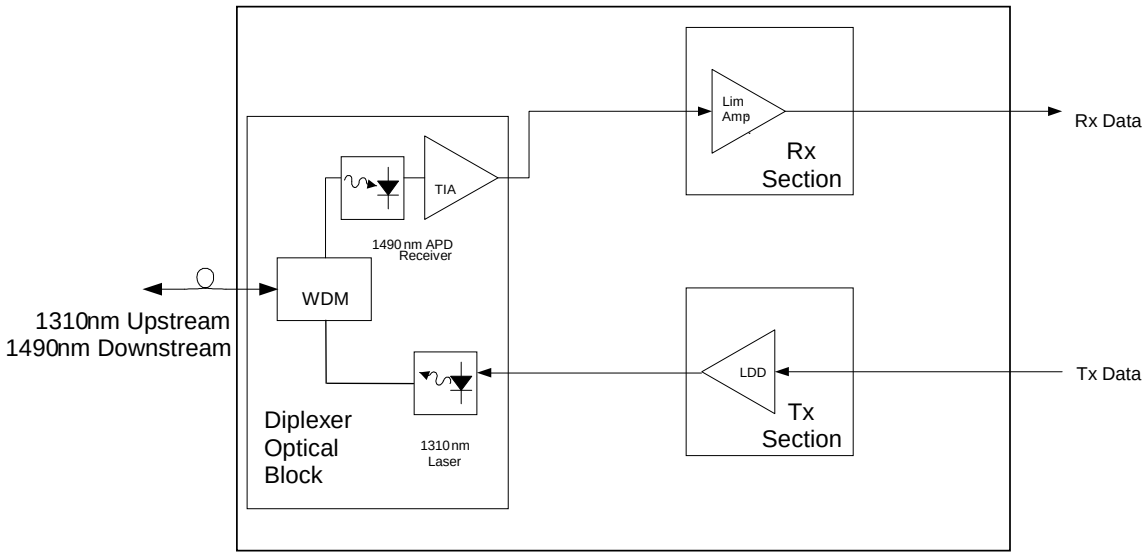
1310/1490 Integrated Diplexer Transceiver

Features

- Single Fiber, Integrated Diplexer Transceiver
- 2x10 SFF pinout supports I^2C digital diagnostics
- Voice/Data FTTx ONT/ONU Applications
- Compliant to FSAN G.984.5 Specifications
- 1244 Mbps Tx, 2488 Mbps Rx Asymmetric Data Rate
- 1310 nm Tx, 1490 nm Rx
- Burst Mode Transmission
- TX Burst Mode Detection, TX_SD
- DDM TX Power
- 28 dB link budget; 20 km reach
- Compliant to IEC-60825 Class 1 laser diode
- SC/APC or SC/UPC fiber connector
- RoHS-6/6 compliant
- Internal Calibration

- Digital Transmitter: A DFB laser diode is employed for upstream transmission at OC-24 (1244Mbps). The optical transmitter includes a back facet photodetector to monitor laser power for UPC control.

- Digital Receiver: An APD with TIA is employed for downstream data reception at OC-48 (2488Mbps). A post amplifier is also included for CML output compatibility.



Diplexer Block Diagram

Absolute Maximum Ratings

Usage of this transceiver shall adhere to the following absolute maximum ratings. Stresses beyond those in Table 1 may cause permanent damage to the unit. These are stress ratings only, and functional operation of the unit at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect unit reliability.

Table 1 - Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit/Conditions
Ambient Storage Temperature	-40	85	ºC
Operating Temperature*	0 -40	70 85	ºC, C-Temp ºC, I-Temp
Operating Humidity Range	10%	90%	non-condensing
ESD Sensitivity (Human Body Model)	-	1000	V
Lead Soldering Temperature	-	260ºC	Maximum 10 sec
Vcc_Rx	-0.4	+4.2	V
Vcc_Tx	-0.4	Vcc_Rx + 1	V

*Operating temp: minimum is ambient, maximum is case.

Module Characteristics

Table 2 - Module Characteristics

Parameter	Minimum	Typical	Maximum	Unit/Conditions
1310nm Tx to 1490nm Rx Crosstalk	-	-	-47	dB
1555nm Rx to 1490nm Isolation	30	-	-	dB
G.984.5 Wavelength Blocking Filter (WBF)	7 7 22 22	- - - -	- - - -	dB, 1441 nm to 1450 nm dB, 1530 nm to 1539 nm dB, 1400 nm to 1441 nm dB, 1539 nm to 1625 nm
Temperature Monitoring Accuracy	-3	-	+3	℃
Voltage Monitoring Accuracy	-3	-	+3	%
Bias Current Monitoring Accuracy	-10	-	+10	%
Total TX and RX Supply Current	-	-	300	mA

Functional Characteristics

The following tables list the performance specifications for the various functional blocks of the integrated optical transceiver module.

Table 3 – Digital Transmitter Specifications

Parameter	Minimum	Typical	Maximum	Unit	Notes
Operating Voltage	3.14	3.30	3.46	V	V_{CC} referenced to GND_Tx
Data Rate	-	1244.16	-	Mbps	
Average Optical Output Power, P_O	0.5	-	5	dBm	
Output Power at Transmit Off	-	-	-50	dBm	
Extinction Ratio	10	-	-	dB	PRBS 2^{23}-1, NRZ, 50% duty cycle
Transmitter Output Eye	G.984.2 Figure 3				
Optical Rise and Fall Time	-	250	-	ps	20% to 80%
Center Wavelength	1290		1330	nm	
Differential Input Voltage	300	-	1800	mVp-p	TXD+/-. Internally DC-coupled
Input Impedance, differential	-	100	-	Ω	
Common-Mode Input Voltage	GND_Tx + 1.4	-	Vcc - (V_{in}/2) - 0.1	V	Internally DC coupled
Tx Burst Enable Time	-	-	12.8	ns	16 bits data @ 1244Mbps
Tx Burst Disable Time	-	-	12.8	ns	16 bits data @ 1244Mbps
Jitter Generation	-	-	0.2	UI	4 kHz to 10 MHz
TX_BEN Input Low	0		0.8	V	
TX_BEN Input High	2.0		Vcc_RX	V	
TX_SD timing “D”			1	µs	See figure 2
TX_SD timing “X”			100	ns	See figure 2
Ttx-sd_startup			3	S	See Figure 3

Refer to Figure 1 which schematically describes the high speed data inputs/outputs of the optical transceiver module.

For CML
Tx/Rx Data

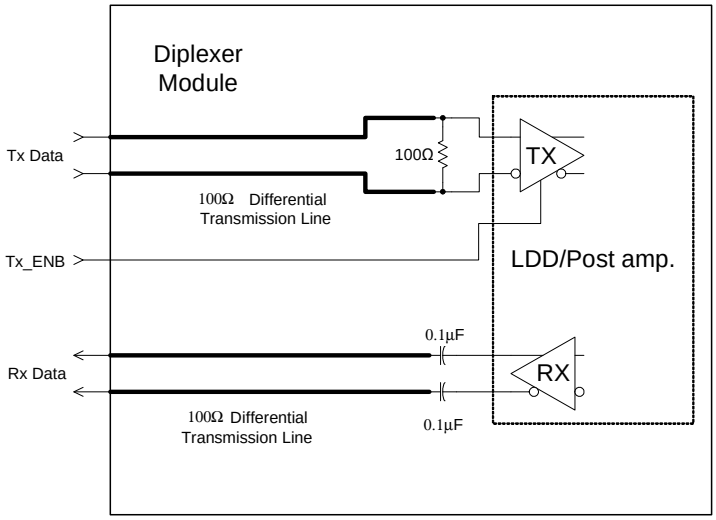


Figure 1 - Schematic representation of the module high speed inputs/outputs

Table 4 – Digital Receiver Specifications

Parameter	Minimum	Typical	Maximum	Unit	Notes
Operating Voltage	3.14	3.30	3.46	V	V_{CC} referenced to GND_RX
Data Rate	-	2488.32	-	Mbps	
Operational Wavelength Range	1480	-	1500	nm	
Received Optical Power	-28	-	-8	dBm	BER≤10^{-10}, PRBS 2^{23}-1, 50% duty cycle
Data Output Rise and Fall Time	-	160	-	ps	20% to 80%
Signal Detect Assertion Level	-	-	-31	dBm	Transition during increasing light
Signal Detect De-Assertion Level	-45	-	-	dBm	Transition during decreasing light
Signal Detect Hysteresis	0.5	-	6	dB	
Differential Output Voltage	300	-	1200	mV	CML output, ac coupled
Signal Detect Output HIGH Voltage	2.4	-	-	V	LVTTL with internal pull up resistor, I_{OH}=400µA. Asserts HIGH when input data amplitude is above threshold.
Signal Detect Output LOW Voltage	-	-	0.6	V	LVTTL. I_{OL}=4mA De-asserts LOW when input data amplitude is below threshold .
RSSI Range	-28	-	-8	dBm	
RSSI Accuracy	-3	-	+3	dB	

Table 5 - Microcontroller Specifications

Parameter	Minimum	Typical	Maximum	Unit	Notes
Operating Voltage	3.14	3.30	3.46	V	
SDA[a]	-	-	-	-	LVTTL, open collector serial data line from the I^{2}C bus to the on board Microcontroller. 100kbps max. data rate.
SCL[b]	-	-	-	-	LVTTL, open collector serial clock line from the I^{2}C bus to the on board Microcontroller.
Reset hold[c]	30	-	-	ms	LVTTL input, internal 50kΩ pull-up. Active Low
Module temperature accuracy	-3	-	+3	°C	Digital diagnostics status monitor module's case temperature.
VCC monitor accuracy	-0.1	-	+0.1	V	Digital diagnostics status monitor of the module's 3.3V bias supply.

[a] I^{2}C SDA and SCL must be open collector or open drain connections.
[b] Clock stretching, as per paragraph 13.2 of the I^{2}C Bus Standard, must be implemented to operate correctly.
[c] Please see Table 6 for the recommended system start-up sequence.

Table 6 – Suggested Start-up Sequence

Step	Action
1	Power up the host system, with the RESET pin pulled to ground via a ≤4.7kΩ resistor.
2	Drive the RESET pin LOW.
3	Ensure power to the unit is on.
4	Drive the RESET pin HIGH to release the unit to become operational.
5	Read byte A2.6E several times. There will be a NACK until the processor is booted, followed by a 01 (DATA READY BAR) until the A2D data is ready, followed by 00 (assuming TX_BEN and TX_FAIL are inactive).
6	The unit is now ready for normal operation.

Pin Definitions

Refer to Table 7 for a description of the function of each I/O pin.

Pin Number	Label	Definition
1	NC	No User Connection
2	NC	No User Connection
3	GND_RX	Digital Rx ground
4	NC	Reserved, No User Connection
5	NC	Reserved, No User Connection
6	GND_RX	Digital Rx Ground
7	Vcc_RX	Digital Rx Vcc
8	RX_SD	Receiver signal detect output, pull up internally. LVTTL. Asserts high when input optical power level is above threshold.
9	RxD-	RX data bar output, CML, AC coupled
10	RxD+	RX data output, CML, AC coupled
11	Vcc_TX	Digital Tx Vcc
12	GND_TX	Digital Tx Ground
13	TX_BEN	Tx BEN, LVTTL Input. Active High (Logic High=TX ON, Logic Low=TX OFF)
14	TxD+	Tx data input, LVPECL or CML. Internally DC coupled.
15	TxD-	Tx data bar input, LVPECL or CML. Internally DC coupled.
16	GND_TX	Digital Tx Ground
17	SCL	I2C Clock input
18	SDA	I2C Data input/output
19	TX_Fault	TX Fault Alarm, LVTTL, TX Fault state=High, TX Normal state=Low.
20	TX_SD	TX Signal Detect, LVTTL, TX Active state=High. See TX_SD diagram. Internal 1KΩ pull-down.

Figure 2 TX_SD timing diagram:

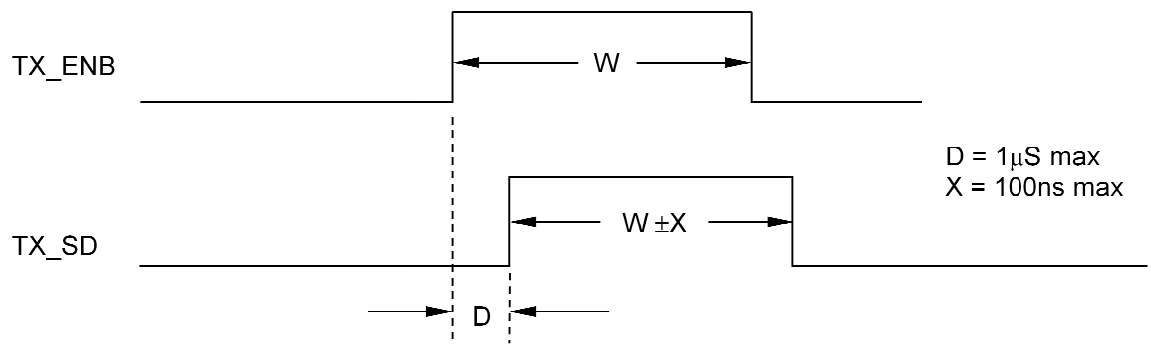
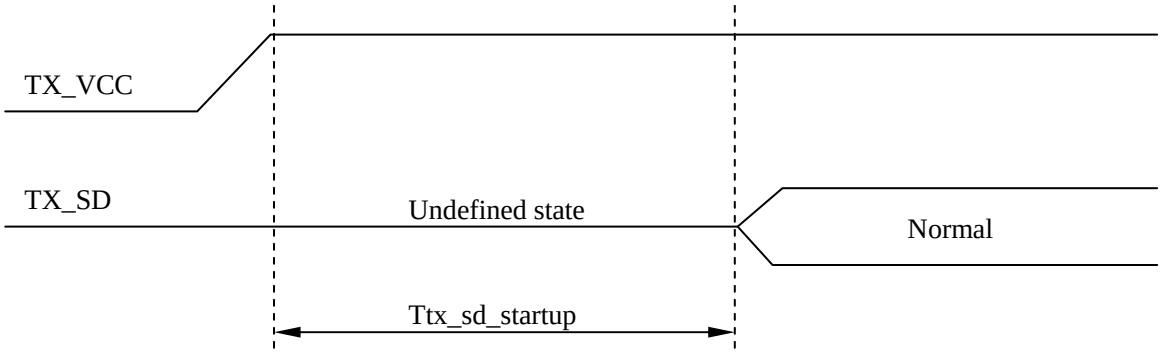
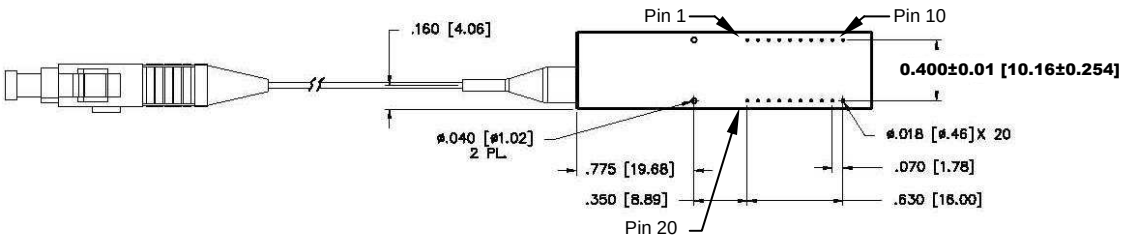
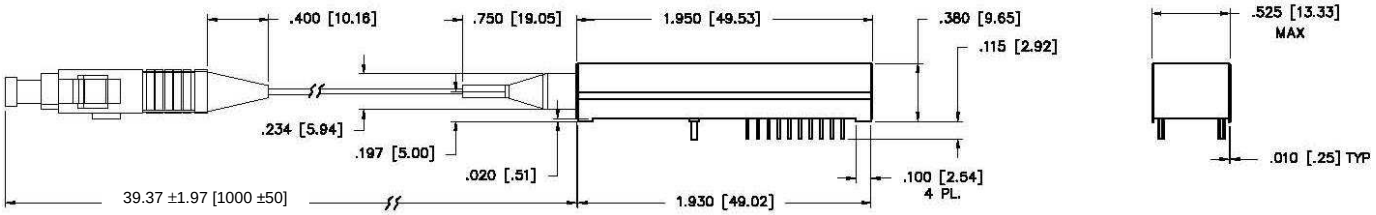


Figure 3 TX_SD startup timing diagram



Package Diagram





EEPROM Memory Content (A0h)

Address	Field Size (Byte)	Name of Field	Hex	Description
0	1	Identifier	02	SFF
1	1	Ext. Identifier	04	
2	1	Connector	0B	Pigtail（SC/UPC）
3-10	8	Transceiver	00 00 00 00 00 00 00 00	not defined
11	1	Encoding	03	NRZ
12	1	BR, Nominal	0D	1.25 Gbps（1.244Gbps）
13	1	Reserved	00	
14	1	Length (9um)-km	14	20(km)
15	1	Length (9um)	C8	200(100m)
16	1	Length (50um)	00	Not Support MMF
17	1	Length (62.5um)	00	Not Support MMF
18	1	Length (Copper)	00	Not Support Copper
19	1	Reserved	00	
20-35	16	Vendor name	Xx	(ASCII)
36	1	Reserved	00	
37-39	3	Vendor OUI	00 00 00	
40-55	16	Vendor PN	xx	(ASCII)
56-59	4	Vendor Rev	xx	(ASCII)
60-61	2	Wavelength	05 1E	1310nm Laser Wavelength
62	1	Reserved	00	
63	1	CC_BASE	xx	Check sum of byte 0-62
64-65	2	Options	00 0A	Supports TX_Fault & TX_SD.
66	1	BR, max	00	
67	1	BR, min	00	
68-83	16	Vendor SN	xx……..xx	ASCII
84-91	8	Date code	xx…….xx	Year,Month,Day
92	1	Diagnostic Monitoring Type	58 or 68	Compliant with SFF-8472 V9.5 Externally Calibrated(0x58) or Internally Calibrated (0x68) Received power measurement type-Average Power
93	1	Enhanced Options	B0	Optional Alarm/warning implemented. Soft TX_FAULT,RX_SD implemented
94	1	SFF-8472 Compliance	02	Diagnostics Compliance(SFF-8472 V9.5)

Address	Field Size (Byte)	Name of Field	Hex	Description
95	1	CC_EXT	xx	Check sum of byte 64-94
96-127	64	Vendor Specific		not defined

EEPROM Memory Content (A2h)

Address	Field Size (Byte)	Bits	Name of Field	Description
00~01	2	ALL	Temp High Alarm Thresholds	MSB at low address,80°C
02~03	2	ALL	Temp Low Alarm Thresholds	MSB at low address,-13°C
04~05	2	ALL	Temp High Warning Thresholds	MSB at low address,75°C
06~07	2	ALL	Temp Low Warning Thresholds	MSB at low address,-8°C
08~09	2	ALL	Voltage High Alarm Thresholds	MSB at low address,3.6V
10~11	2	ALL	Voltage Low Alarm Thresholds	MSB at low address,3.0V
12~13	2	ALL	Voltage High Warning Thresholds	MSB at low address,3.5V
14~15	2	ALL	Voltage Low Warning Thresholds	MSB at low address,3.1V
16~17	2	ALL	Bias High Alarm Thresholds	MSB at low address,90mA
18~19	2	ALL	Bias Low Alarm Thresholds	MSB at low address,0mA
20~21	2	ALL	Bias High Warning Thresholds	MSB at low address,70mA
22~23	2	ALL	Bias Low Warning Thresholds	MSB at low address,0mA
24~25	2	ALL	TX Power High Alarm Thresholds	MSB at low address,6.0dBm
26~27	2	ALL	TX Power Low Alarm Thresholds	MSB at low address,-0.5dBm
28~29	2	ALL	TX Power High Warning Thresholds	MSB at low address,5.5dBm
30~31	2	ALL	TX Power Low Warning Thresholds	MSB at low address,0.0dBm
32~33	2	ALL	RX Power High Alarm Thresholds	MSB at low address,-7.0dBm
34~35	2	ALL	RX Power Low Alarm Thresholds	MSB at low address,-28dBm
36~37	2	ALL	RX Power High Warning Thresholds	MSB at low address,-8.0dBm
38~39	2	ALL	RX Power Low Warning Thresholds	MSB at low address,-27dBm
40~55	16	ALL	Reserved	Reserved
56~59	4	ALL	Rx_PWR(4)	Single precision floating point calibration data - Rx optical power. Bit 7 of byte 56 is MSB. Bit 0 of byte 59 is LSB. Rx_PWR (4) should be set to zero for “internally calibrated” devices.

Address	Field Size (Byte)	Bits	Name of Field	Description
60~63	4	ALL	Rx_PWR(3)	Single precision floating point calibration data - Rx optical power. Bit 7 of byte 60 is MSB. Bit 0 of byte 63 is LSB. Rx_PWR (3) should be set to zero for “internally calibrated” devices.
64~67	4	ALL	Rx_PWR(2)	Single precision floating point calibration data, Rx optical power. Bit 7 of byte 64 is MSB, bit 0 of byte 67 is LSB. Rx_PWR (2) should be set to zero for “internally calibrated” devices.
68~71	4	ALL	Rx_PWR(1)	Single precision floating point calibration data, Rx optical power. Bit 7 of byte 68 is MSB, bit 0 of byte 71 is LSB. Rx_PWR (1) should be set to 1 for “internally calibrated” devices.
72~75	4	ALL	Rx_PWR(0)	Single precision floating point calibration data, Rx optical power. Bit 7 of byte 72 is MSB, bit 0 of byte 75 is LSB. Rx_PWR (0) should be set to zero for “internally calibrated” devices.
76~77	2	ALL	Tx_I(Slope)	Fixed decimal (unsigned) calibration data, laser bias current. Bit 7 of byte 76 is MSB, bit 0 of byte 77 is LSB. For “internally calibrated” devices, Tx_I (Slope) should be set to 1.
78~79	2	ALL	Tx_I(Offset)	Fixed decimal (signed two’s complement) calibration data, laser bias current. Bit 7 of byte 78 is MSB, bit 0 of byte 79 is LSB. For “internally calibrated” devices, Tx_I (Offset) should be set to zero.
80~81	2	ALL	Tx_PWR(Slope)	Fixed decimal (unsigned) calibration data, transmitter coupled output power. Bit 7 of byte 80 is MSB, bit 0 of byte 81 is LSB.For “internally calibrated” devices, Tx_PWR (Slope) should be set to 1.

Address	Field Size (Byte)	Bits	Name of Field	Description
82~83	2	ALL	Tx_PWR(Offset)	Fixed decimal (signed two's complement) calibration data, transmitter coupled output power. Bit 7 of byte 82 is MSB, bit 0 of byte 83 is LSB. For "internally calibrated" devices, Tx_PWR (Offset) should be set to zero.
84~85	2	ALL	T (Slope)	Fixed decimal (unsigned) calibration data, internal module temperature. Bit 7 of byte 84 is MSB, bit 0 of byte 85 is LSB. For "internally calibrated" devices, T (Slope) should be set to 1.
86~87	2	ALL	T (Offset)	Fixed decimal (signed two's complement) calibration data, internal module temperature. Bit 7 of byte 86 is MSB, bit 0 of byte 87 is LSB.For "internally calibrated" devices, T (Offset) should be set to zero.
88~89	2	ALL	V (Slope)	Fixed decimal (unsigned) calibration data, internal module supply voltage. Bit 7 of byte 88 is MSB, bit 0 of byte 89 is LSB. For "internally calibrated" devices, V(Slope)should be set to 1.
90~91	2	ALL	V (Offset)	Fixed decimal (signed two's complement) calibration data, internal module supply voltage. Bit 7 of byte 90 is MSB. Bit 0 of byte 91 is LSB. For "internally calibrated" devices, V(Offset) should be set to zero.
92~94	3	ALL	Reserved	Reserved
95	1	ALL	Checksum	Byte 95 contains the low order 8 bits of the sum of bytes 0 – 94.
96	1	ALL	Temperature MSB	Internally measured module temperature.
97	1	ALL	Temperature LSB	
98	1	ALL	Vcc MSB	Internally measured supply voltage in transceiver.
99	1	ALL	Vcc LSB	

Address	Field Size (Byte)	Bits	Name of Field	Description
100	1	ALL	TX Bias MSB	Internally measured TX Bias Current.
101	1	ALL	TX Bias LSB	
102	1	ALL	TX Power MSB	Measured TX output power.
103	1	ALL	TX Power LSB	
104	1	ALL	RX Power MSB	Measured RX input power.
105	1	ALL	RX Power LSB	Measured RX input power.
106~109	4	ALL	Reserved	Reserved
110	1	7	Reserved	Reserved
		6	Soft TX Disable	Read/write bit that allows software disable of laser. Writing '1' disables laser.
		5	Reserved	Reserved
		4	Reserved	Reserved
		3	Reserved	Reserved
		2	TX Fault	Tx Fail Status: 1=TX Fail; 0=TX Normal
		1	LOS	Signal Detect Status. Active High.
		0	Reserved	Reserved
111	1	ALL	Reserved	Reserved
112	1	7	Temp High Alarm	Set when internal temperature exceeds high alarm level.
		6	Temp Low Alarm	Set when internal temperature is below low alarm level.
		5	Vcc High Alarm	Set when internal supply voltage exceeds high alarm level.
		4	Vcc Low Alarm	Set when internal supply voltage is below low alarm level.
		3	TX Bias High Alarm	Set when TX Bias current exceeds high alarm level.
		2	TX Bias Low Alarm	Set when TX Bias current is below low alarm level.
		1	TX Power High Alarm	Set when TX output power exceeds high alarm level.
		0	TX Power Low Alarm	Set when TX output power is below low alarm level.
113	1	7	RX Power High Alarm	Set when Received Power exceeds high alarm level.

Address	Field Size (Byte)	Bits	Name of Field	Description
		6	RX Power Low Alarm	Set when Received Power is below low alarm level.
		5	Reserved	Reserved
		4	Reserved	Reserved
		3	Reserved	Reserved
		2	Reserved	Reserved
		1	Reserved	Reserved
		0	Reserved	Reserved
114	1	ALL	Reserved	Reserved
115	1	ALL	Reserved	Reserved
116	1	7	Temp High Warning	Set when internal temperature exceeds high warning level.
		6	Temp Low Warning	Set when internal temperature is below low warning level.
		5	Vcc High Warning	Set when internal supply voltage exceeds high warning level.
		4	Vcc Low Warning	Set when internal supply voltage is below low warning level.
		3	TX Bias High Warning	Set when TX Bias current exceeds high warning level.
		2	TX Bias Low Warning	Set when TX Bias current is below low warning level.
		1	TX Power High Warning	Set when TX output power exceeds high warning level.
		0	TX Power Low Warning	Set when TX output power is below low warning level.
117	1	7	RX Power High Warning	Set when Received Power exceeds high warning level.
		6	RX Power Low Warning	Set when Received Power is below low warning level.
		5	Reserved	Reserved
		4	Reserved	Reserved
		3	Reserved	Reserved
		2	Reserved	Reserved
		1	Reserved	Reserved
		0	Reserved	Reserved
118	1	ALL	Reserved	Reserved

Address	Field Size (Byte)	Bits	Name of Field	Description
119	1	ALL	Reserved	Reserved
120-127	8	ALL	Vendor Specific	Vendor Specific
128-247	120	ALL	User EEPROM	User writable EEPROM
248-255	8	ALL	Vendor Specific	Vendor Specific

DDM complies with SFF-8472-2004 Ver9.5, external Calibration or Internal Calibration.

Ordering Information

Table 8 - Ordering Information

	Connector		Temperature Range	Digital Diagnostic	Design Revision	Customer Specific
SF	**X**	**-34-24T-HP-**	**X**	**D**	**H**	**-XX**
	A = APC		**C** = Commercial Temp (0 to 70℃)	**D** = Diagnostic		
	U = UPC		**I** = Industrial Temp (-40 to 85℃)			

Example: **SFA-34-24T-HP-CDH-XX** = Transceiver with APC connector, C-Temp, Diagnostic, Customer code XX.

Table 9 - Device Handling/ESD Protection

The devices are static sensitive and may easily be damaged if care is not taken during handling. The following handling practices are recommended.	
1	Devices should be handled on benches with conductive and grounding surfaces.
2	All personnel, test equipment and tools shall be grounded.
3	Do not handle the devices by their leads.
4	Store devices in protective foam or carriers.
5	Avoid the use of non-conductive plastics, rubber, or silk in the area where the devices are handled
6	All modules shall be packaged in materials that are anti-static to protect against adverse electrical environments.
7	Avoid applications of any voltage higher than maximum rated voltages to this part. For proper operation, any VIN or VOUT should be constrained to the range GND ≤ (VIN or VOUT) ≤ VCC. Unused inputs must always be tied to an appropriate logic voltage (e.g. either GND or VCC). Unused outputs must be left open.

Warnings

Handling Precautions: This device is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.

Laser Safety: Radiation emitted by laser devices can be dangerous to human eyes. Avoid eye exposure to direct or indirect radiation.

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