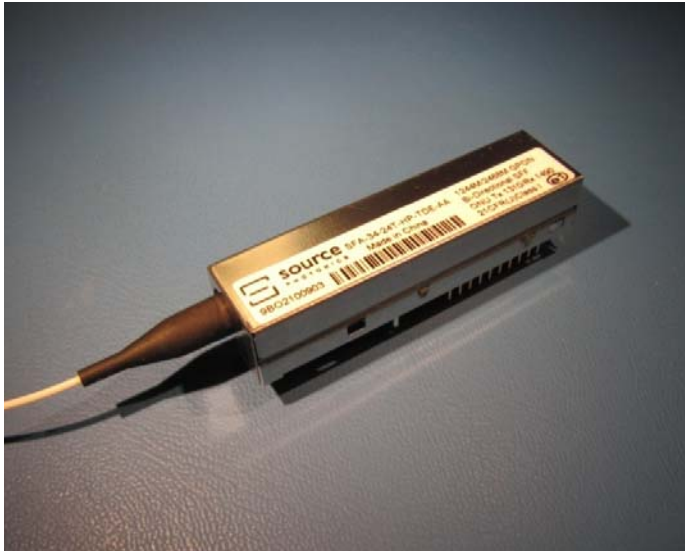


1310/1490 Integrated Diplexer Transceiver

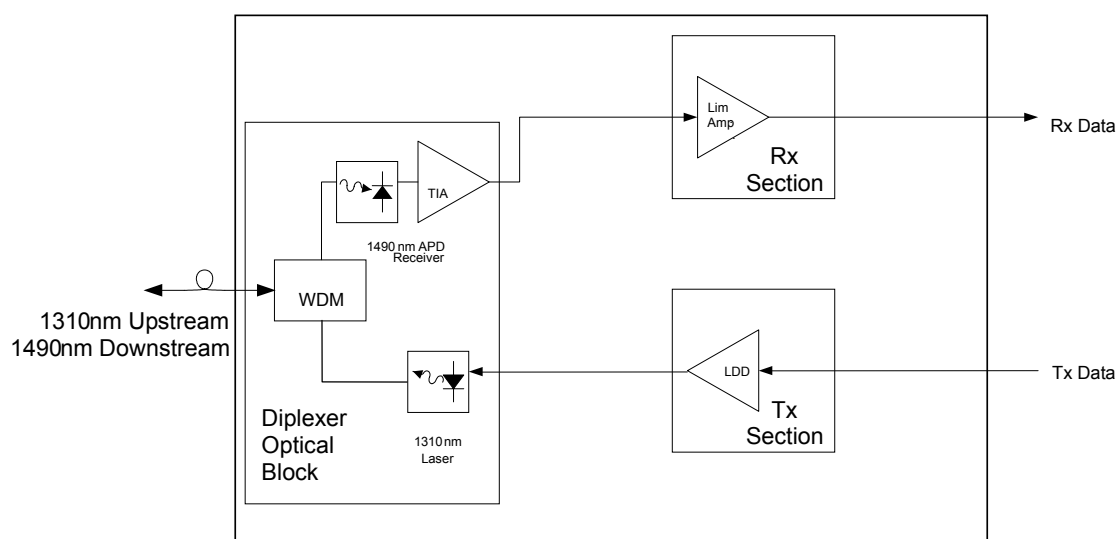


Features

- Single Fiber, Integrated Diplexer Transceiver
- 2x10 SFF pinout supports I²C digital diagnostics
- Voice/Data FTTx ONT/ONU Applications
- Compliant to FSAN G.984.5 Specifications
- 1244 Mbps Tx, 2488 Mbps Rx Asymmetric Data Rate
- 1310 nm Tx, 1490 nm Rx
- Burst Mode Transmission
- TX Burst Mode Detection, TX_SD
- DDM TX Power
- 28 dB link budget; 20 km reach
- Compliant to IEC-60825 Class 1 laser diode
- SC/APC or SC/UPC fiber connector
- RoHS compliant
- Internal Calibration

- **Digital Transmitter:** A DFB laser diode is employed for upstream transmission at OC-24 (1244Mbps). The optical transmitter includes a back facet photodetector to monitor laser power for UPC control.

- **Digital Receiver:** An APD with TIA is employed for downstream data reception at OC-48 (2488Mbps). A post amplifier is also included for CML output compatibility.



Diplexer Block Diagram

Absolute Maximum Ratings

Usage of this transceiver shall adhere to the following absolute maximum ratings. Stresses beyond those in Table 1 may cause permanent damage to the unit. These are stress ratings only, and functional operation of the unit at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect unit reliability.

Table 1 - Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit/Conditions
Ambient Storage Temperature	-40	85	°C
Operating Temperature*	0	70	°C, C-Temp
	-40	85	°C, I-Temp
Operating Humidity Range	10%	90%	non-condensing
ESD Sensitivity (Human Body Model)	-	1000	V
Lead Soldering Temperature	-	260°C	Maximum 10 sec
Vcc_Rx	-0.4	+4.2	V
Vcc_Tx	-0.4	Vcc_Rx + 1	V

*Operating temp: minimum is ambient, maximum is case.

Module Characteristics

Table 2 - Module Characteristics

Parameter	Minimum	Typical	Maximum	Unit/Conditions
1310nm Tx to 1490nm Rx Crosstalk	-	-	-47	dB
1555nm Rx to 1490nm Isolation	30	-	-	dB
G.984.5 Wavelength Blocking Filter (WBF), X/S	7	-	-	dB, 1441 nm to 1450 nm
	7	-	-	dB, 1530 nm to 1539 nm
	22	-	-	dB, 1400 nm to 1441 nm
	22	-	-	dB, 1539 nm to 1625 nm
Temperature Monitoring Accuracy	-3	-	+3	°C
Voltage Monitoring Accuracy	-3	-	+3	%
Bias Current Monitoring Accuracy	-10	-	+10	%
Total TX and RX Supply Current	-	-	350	mA

Functional Characteristics

The following tables list the performance specifications for the various functional blocks of the integrated optical transceiver module.

Table 3 – Digital Transmitter Specifications

Parameter	Minimum	Typical	Maximum	Unit	Notes
Operating Voltage	3.14	3.30	3.46	V	V _{CC} referenced to GND_Tx
Data Rate	-	1244.16	-	Mbps	
Average Optical Output Power, P _O	0.5	-	5	dBm	
Output Power at Transmit Off	-	-	-50	dBm	
Extinction Ratio	10	-	-	dB	PRBS 2 ²³ -1, NRZ, 50% duty cycle
Transmitter Output Eye	G.984.2 Figure 3				
Optical Rise and Fall Time	-	250	-	ps	20% to 80%
Center Wavelength	1290		1330	nm	
Differential Input Voltage	300	-	1800	mVp-p	TXD+/- Internally DC-coupled
Input Impedance, differential	-	100	-	Ω	
Common-Mode Input Voltage	GND_Tx + 1.4	-	V _{CC} - (V _{in} /2) - 0.1	V	Internally DC coupled
Tx Burst Enable Time	-	-	12.8	ns	16 bits data @ 1244Mbps
Tx Burst Disable Time	-	-	12.8	ns	16 bits data @ 1244Mbps
Jitter Generation	-	-	0.2	UI	4 kHz to 10 MHz
TX_BEN Input Low	0		0.8	V	
TX_BEN Input High	2.0		V _{CC_RX}	V	
TX_SD timing "D"			1	μs	See figure 3
TX_SD timing "X"			100	ns	See figure 3
Ttx-sd_startup			3	S	See Figure 4

Refer to Figure 1 which schematically describes the timing parameter definition in burst mode sequence.

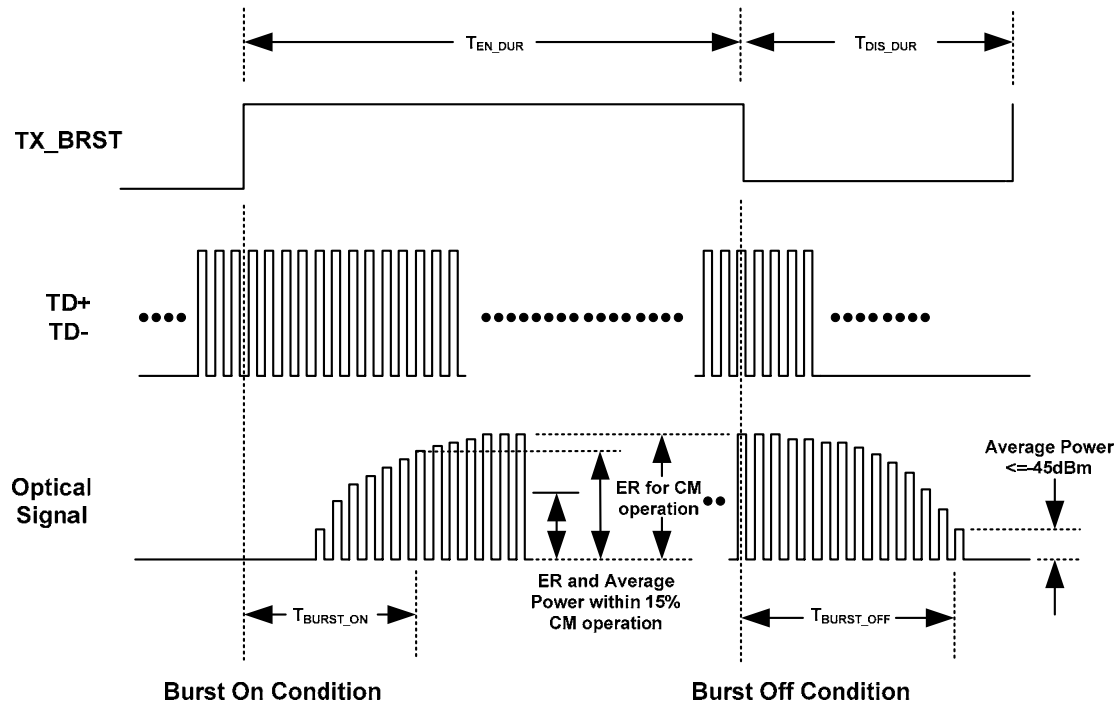


Figure 1 - Timing Parameter Definition in Burst Mode Sequence

Table 4 – Digital Receiver Specifications

Parameter	Minimum	Typical	Maximum	Unit	Notes
Operating Voltage	3.14	3.30	3.46	V	V_{CC} referenced to GND_RX
Data Rate	-	2488.32	-	Mbps	
Operational Wavelength Range	1480	-	1500	nm	
Received Optical Power	-28	-	-8	dBm	$BER \leq 10^{-10}$, PRBS $2^{23}-1$, 50% duty cycle
Data Output Rise and Fall Time	-	160	-	ps	20% to 80%
Signal Detect Assertion Level	-	-	-31	dBm	Transition during increasing light
Signal Detect De-Assertion Level	-45	-	-	dBm	Transition during decreasing light
Signal Detect Hysteresis	0.5	-	6	dB	
Differential Output Voltage	300	-	1200	mV	CML output, ac coupled

Parameter	Minimum	Typical	Maximum	Unit	Notes
Signal Detect Output HIGH Voltage	2.4	-	-	V	LVTTTL with internal pull up resistor, $I_{OH}=400\mu A$. Asserts HIGH when input data amplitude is above threshold.
Signal Detect Output LOW Voltage	-	-	0.6	V	LVTTTL. $I_{OL}=4mA$ De-asserts LOW when input data amplitude is below threshold .
RSSI Range	-28	-	-8	dBm	
RSSI Accuracy	-3	-	+3	dB	

Table 5 - Microcontroller Specifications

Parameter	Minimum	Typical	Maximum	Unit	Notes
Operating Voltage	3.14	3.30	3.46	V	
SDA ^a	-	-	-	-	LVTTTL, open collector serial data line from the I ² C bus to the on board Microcontroller. 100kbps max. data rate.
SCL	-	-	-	-	LVTTTL, open collector serial clock line from the I ² C bus to the on board Microcontroller.
Reset hold	30	-	-	ms	LVTTTL input, internal 50k Ω pull-up. Active Low
Module temperature accuracy	-3	-	+3	°C	Digital diagnostics status monitor module's case temperature.
VCC monitor accuracy	-0.1	-	+0.1	V	Digital diagnostics status monitor of the module's 3.3V bias supply.

^a I²C SDA and SCL must be open collector or open drain connections.

Pin Definitions

Refer to Table 6 for a description of the function of each I/O pin.

Table 6 - Module Pin Definitions

Pin Number	Label	Definition
1	NC	No User Connection
2	GND_RX	Digital Rx ground
3	GND_RX	Digital Rx ground
4	NC	Reserved, No User Connection
5	NC	Reserved, No User Connection
6	GND_RX	Digital Rx Ground
7	Vcc_RX	Digital Rx Vcc
8	RX_SD	Receiver signal detect output, pull up internally. LVTTTL. Asserts high when input optical power level is above threshold.
9	RxD-	RX data bar output, CML, AC coupled
10	RxD+	RX data output, CML, AC coupled
11	Vcc_TX	Digital Tx Vcc
12	GND_TX	Digital Tx Ground
13	TX_BEN	Tx BEN, LVTTTL Input. Active High (Logic High=TX ON, Logic Low=TX OFF)
14	TxD+	Tx data input, LVPECL or CML. Internally DC coupled.
15	TxD-	Tx data bar input, LVPECL or CML. Internally DC coupled.
16	GND_TX	Digital Tx Ground
17	SCL	I2C Clock input
18	SDA	I2C Data input/output
19	TX_Fault	TX Fault Alarm, LVTTTL, TX Fault state=High, TX Normal state=Low.
20	TX_SD	TX Signal Detect, LVTTTL, TX Active state=High. See TX_SD diagram. Internal 1KΩ pull-down.

Figure 3 TX_SD timing diagram:

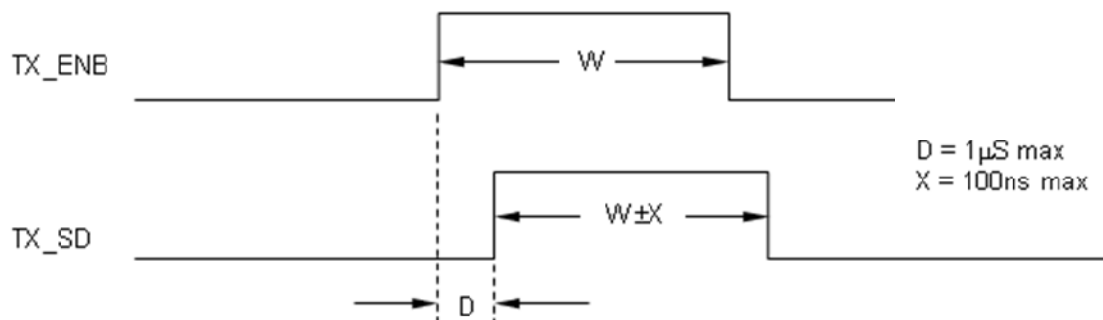
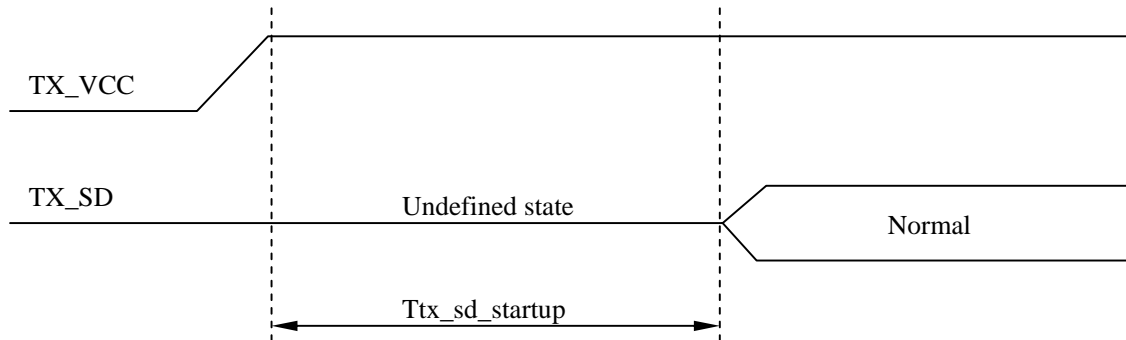
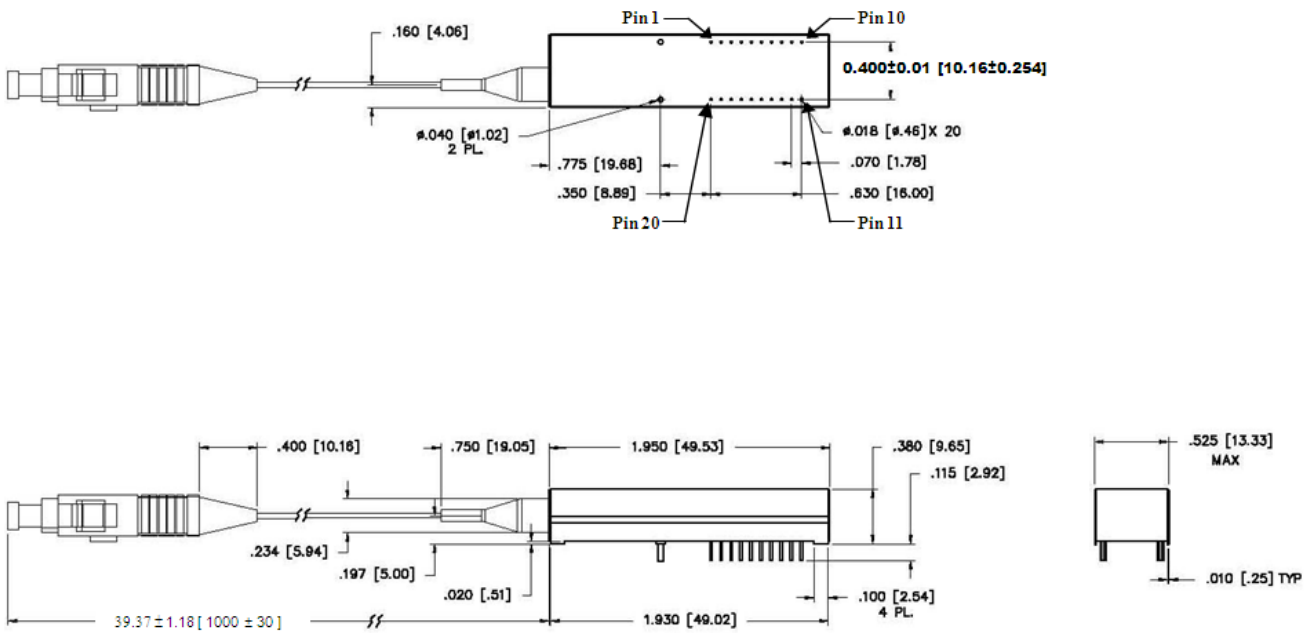


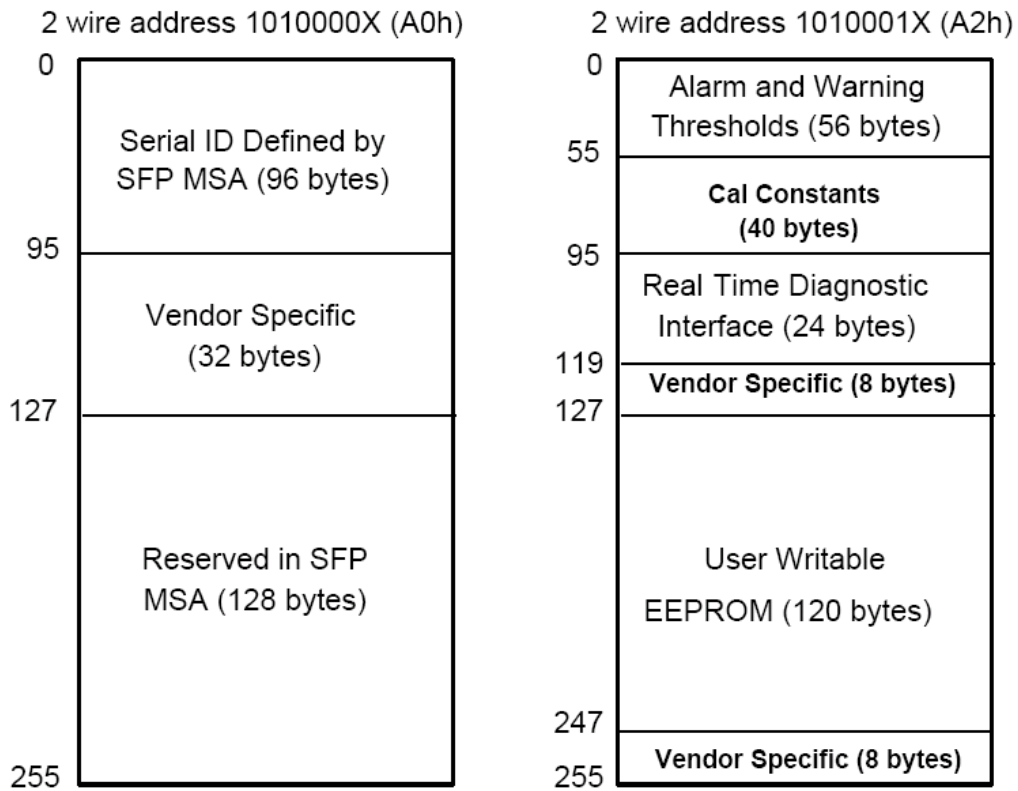
Figure 4 TX_SD startup timing diagram



Mechanical Diagram



EEPROM information



EEPROM Memory Content (A0h)

Addr.	Field Size (Bytes)	Name of Field	Hex	Description
0	1	Identifier	02	Module/connector soldered to motherboard
1	1	Ext. Identifier	04	MOD4
2	1	Connector	0B	Optical Pigtail
3-10	8	Transceiver	00 00 00 00 00 00 00 00	
11	1	Encoding	03	NRZ
12	1	BR, Nominal	0D	1.244Gbps

13	1	Reserved	00	
14	1	Length (9um)-km	14	20(km)
15	1	Length (9um)	C8	200(100m)
16	1	Length (50um)	00	Not Support MMF
17	1	Length (62.5um)	00	Not Support MMF
18	1	Length (Copper)	00	Not Support Copper
19	1	Reserved	00	
20-35	16	Vendor name	53 4F 55 52 43 45 50 48 4F 54 4F 4E 49 43 53 20	"SOURCEPHOTONICS "(ASC II)
36	1	Reserved	00	
37-39	3	Vendor OUI	00 00 00	
40-55	16	Vendor PN	53 46 xx 33 34 32 34 54 48 50 yy 44 46 41 20 20	"SFX3424THPYDFA" (ASCII) X=A; xx=41; X=U; xx=55; Y=C; yy=43; Y=T; yy=54;
56-59	4	Vendor Rev	xx xx 20 20	ASCII("31 30 20 20" means 1.0 Revision)
60-61	2	Wavelength	05 1E	1310nm Laser Wavelength
62	1	Reserved	00	
63	1	CC_BASE	xx	Check sum of byte 0-62
64-65	2	Options	00 0C	Rx_SD, Tx_Fault
66	1	BR, max	00	
67	1	BR, min	00	
68-83	16	Vendor SN	xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx	ASCII
84-91	8	Date code	xx xx xx xx xx xx 20 20	Year(2 bytes),Month(2 bytes), Day(2 bytes)
92	1	Diagnostic Monitoring Type	68	Compliant with SFF-8472 V9.5 Internally Calibrated Received power measurement type -Average Power
93	1	Enhanced Options	B0	Optional Alarm/warning Flags Implemented; Tx_Fault;Rx_Los
94	1	SFF-8472 Compliance	02	Diagnostics Compliance(SFF-8472 V9.5)
95	1	CC_EXT	xx	Check sum of byte 64-94
96-255	64	Vendor Specific		

EEPROM Memory Content (A2h)

Addr.		Field Size (Bytes)	Name of Field	Hex	Description
0	00	2	Temp High Alarm	64 00(I temp) 50 00(C temp)	100°C (I temp) 80°C (C temp)
2	02	2	Temp Low Alarm	CE 00(I temp) F3 00(C temp)	-50°C (I temp) -13°C (C temp)
4	04	2	Temp High Warning	5A 00 (I temp) 4B 00(C temp)	90°C (I temp) 75°C (C temp)
6	06	2	Temp Low Warning	D8 00(I temp) F8 00(C temp)	-40°C (I temp) -8°C (C temp)
8	08	2	Voltage High Alarm	8C A0	3.6V
10	0A	2	Voltage Low Alarm	75 30	3.0V
12	0C	2	Voltage High Warning	88 B8	3.5V
14	0E	2	Voltage Low Warning	79 18	3.1V
16	10	2	Bias High Alarm	AF C8	90mA
18	12	2	Bias Low Alarm	00 00	0mA
20	14	2	Bias High Warning	88 B8	70mA
22	16	2	Bias Low Warning	00 00	0mA
24	18	2	TX Power High Alarm	9B 82	6dBm
26	1A	2	TX Power Low Alarm	22 D0	-0.5dBm
28	1C	2	TX Power High Warning	7B 86	5dBm
30	1E	2	TX Power Low Warning	2B D4	0.5dBm
32	20	2	RX Power High Alarm	07 CB	-7dBm
34	22	2	RX Power Low Alarm	00 0F	-28dBm
36	24	2	RX Power High Warning	06 30	-8dBm
38	26	2	RX Power Low Warning	00 14	-27dBm
40	28	16	Reserved	00...000	Reserved
56	38	4	RX_PWR(4) Calibration	00 00 00 00	4th order RSSI calibration coefficient
60	3C	4	RX_PWR(3) Calibration	00 00 00 00	3rd order RSSI calibration coefficient
64	40	4	RX_PWR(2) Calibration	00 00 00 00	2nd order RSSI calibration coefficient
68	44	4	RX_PWR(1) Calibration	3F 80 00 00	1st order RSSI calibration coefficient
72	48	4	RX_PWR(0) Calibration	00 00 00 00	0th order RSSI calibration coefficient
76	4C	2	TX_I(Slope) Calibration	01 00	Slope for Bias calibration
78	4E	2	TX_I(Offset) Calibration	00 00	Offset for Bias calibration
80	50	2	TX_PWR(Slope) Calibration	01 00	Slope for TX Power calibration
82	52	2	TX_PWR(Offset) Calibration	00 00	Offset for TX Power calibration
84	54	2	T(Slope) Calibration	01 00	Slope for Temperature calibration

86	56	2	T(Offset) Calibration	00 00	Offset for Temperature calibration, in units of 256ths C
88	58	2	V(Slope) Calibration	01 00	Slope for VCC calibration
90	5A	2	V(Offset) Calibration	00 00	Offset for VCC calibration
92	5C	3	Reserved	00 00 00	Reserved
95	5F	1	Checksum	xx	Checksum
96	60	2	Transceiver Temperature	xx xx	Temperature in C/256
98	62	2	Supply Voltage	xx xx	Vcc
100	64	2	TX Bias Current	xx xx	BIASMON
102	66	2	TX Optical Output Power	xx xx	Back facet monitor
104	68	2	RX Optical Input Power	xx xx	RSSI
106	6A	2	Reserved	00 00	Reserved
108	6C	2	Reserved	00 00	Reserved
110	6E.7	1bit	TX_DIS State	x	Soft TX disable state
	6E.6	1bit	Soft TX Disable	x	Write bit that allows software disable laser output.
	6E.5	1bit	Reserved.	0	Reserved
	6E.4	1bit	Rate Select State	0	NOT SUPPORTED.
	6E.3	1bit	Rate Select	0	NOT SUPPORTED.
	6E.2	1bit	TX_FAULT	x	Digital state of the TX Fault Output
	6E.1	1bit	Rx LOS	x	Digital state of the Rx LOS Output
	6E.0	1bit	Data Ready Bar	x	Indicates transceiver has achieved power up and data is ready.
111	6F.7	1bit	Reserved	0	Reserved
	6F.6	1bit	Reserved	0	Reserved
	6F.5	1bit	Reserved	0	Reserved
	6F.4	1bit	Reserved	0	Reserved
	6F.3	1bit	Reserved	0	Reserved
	6F.2	1bit	Reserved	x	Reserved
	6F.1	1bit	Reserved	0	Reserved
	6F.0	1bit	Reserved	x	Reserved
112	70.7	1bit	Temperature too high alarm	x	Temperature too high alarm
	70.6	1bit	Temperature too low alarm	x	Temperature too low alarm
	70.5	1bit	VCC too high alarm	x	VCC too high alarm
	70.4	1bit	VCC too low alarm	x	VCC too low alarm
	70.3	1bit	BIASMON too high alarm	x	BIASMON too high alarm
	70.2	1bit	BIASMON too low alarm	x	BIASMON too low alarm
	70.1	1bit	TX Power too high alarm	x	TX Power too high alarm

	70.0	1bit	TX Power too low alarm	x	TX Power too low alarm
113	71.7	1bit	RX Power too high alarm	x	RX Power too high alarm
	71.6	1bit	RX Power too low alarm	x	RX Power too low alarm
	71.5	1bit	Reserved interrupt status bit	x	Reserved interrupt status bit
	71.4	1bit	Reserved interrupt status bit	x	Reserved interrupt status bit
	71.3	1bit	Reserved interrupt status bit	x	Reserved interrupt status bit
	71.2	1bit	Reserved interrupt status bit	x	Reserved interrupt status bit
	71.1	1bit	Reserved interrupt status bit	x	Reserved interrupt status bit
	71.0	1bit	Reserved interrupt status bit	x	Reserved interrupt status bit
114	72	1	Reserved	00	Reserved
115	73	1	Reserved	00	Reserved
116	74.7	1bit	Temperature too high warning	x	Temperature too high warning
	74.6	1bit	Temperature too low warning	x	Temperature too low warning
	74.5	1bit	VCC too high warning	x	VCC too high warning
	74.4	1bit	VCC too low warning	x	VCC too low warning
	74.3	1bit	BIASMON too high warning	x	BIASMON too high warning
	74.2	1bit	BIASMON too low warning	x	BIASMON too low warning
	74.1	1bit	TX Power too high warning	x	TX Power too high warning
	74.0	1bit	TX Power too low warning	x	TX Power too low warning
117	75.7	1bit	RX Power too high warning	x	RX Power too high warning
	75.6	1bit	RX Power too low warning	x	RX Power too low warning
	75.5	1bit	Reserved interrupt status bit	0	Reserved interrupt status bit
	75.4	1bit	Reserved interrupt status bit	0	Reserved interrupt status bit
	75.3	1bit	Reserved interrupt status bit	0	Reserved interrupt status bit
	75.2	1bit	Reserved interrupt status bit	0	Reserved interrupt status bit
	75.1	1bit	Reserved interrupt status bit	0	Reserved interrupt status bit
	75.0	1bit	Reserved interrupt status bit	0	Reserved interrupt status bit
118	76	1	Reserved	00	Reserved
119	77	1	Reserved	00	Reserved
120	78	8	Vendor Specific	00 00 00 00 00 00 00 00	Vendor Specific

Ordering Information

Table 7 - Ordering Information

	Connector		Temperature Range	Digital Diagnostic	RoHS status	Design Revision
SF	X	-34-24T-HP-	X	D	F	H
	A = APC		C = Commercial Temp (0 to 70°C)	D = Diagnostic	RoHS compliant, lead free solder	
	U = UPC		T = Industrial Temp (-40 to 85°C)			

Example: **SFA-34-24T-HP-CDFH** = Transceiver with APC connector, C-Temp, Diagnostic.

Table 8 - Device Handling/ESD Protection

The devices are static sensitive and may easily be damaged if care is not taken during handling. The following handling practices are recommended.

1	Devices should be handled on benches with conductive and grounding surfaces.
2	All personnel, test equipment and tools shall be grounded.
3	Do not handle the devices by their leads.
4	Store devices in protective foam or carriers.
5	Avoid the use of non-conductive plastics, rubber, or silk in the area where the devices are handled
6	All modules shall be packaged in materials that are anti-static to protect against adverse electrical environments.
7	Avoid applications of any voltage higher than maximum rated voltages to this part. For proper operation, any VIN or VOUT should be constrained to the range $GND \leq (VIN \text{ or } VOUT) \leq VCC$. Unused inputs must always be tied to an appropriate logic voltage (e.g. either GND or VCC). Unused outputs must be left open.

Warnings

Handling Precautions: This device is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.

Laser Safety: Radiation emitted by laser devices can be dangerous to human eyes. Avoid eye exposure to direct or indirect radiation.

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